Electronic Version
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Claims

[c1] 1. A method for fabricating a vertical transistor DRAM device, comprising:
providing a semiconductor substrate comprising a vertical transistor memory array region, a support region, and a transition region between the vertical transistor memory array region and the support region, wherein the vertical transistor memory array region comprises a plurality of vertical transistor memory cells and a plurality of array active areas, the support region comprises a plurality of support active areas isolated from each other by shallow trench isolation regions, and wherein a first pad oxide and a first pad nitride are formed on each of the array active areas, and a second pad oxide and second pad nitride are formed on each of the support active areas;
depositing a protective dielectric layer over the semiconductor substrate;
coating and patterning an etch array (EA) photoresist layer on the protective dielectric layer, so that the EA photoresist layer masking the support region and a portion of the transition region;
using the EA photoresist layer as an etching mask and

etching the protective dielectric layer to expose the first pad nitride in the vertical transistor memory array region;

stripping the EA photoresist layer;

using the protective dielectric layer to protect the second pad nitride in the support region and removing the first pad nitride in the vertical transistor memory array region to form recesses on the array active areas;

forming spacers on walls of the recesses on the array active areas;

depositing a dielectric layer covering the protective dielectric layer on the support region, the vertical transistor memory array region, and the transition region, and the dielectric layer filling the recesses; and

performing a chemical mechanical polishing (CMP) process to polish the dielectric layer and the protective layer on the support region using the second pad nitride as a polishing stop layer.

[c2] 2. The method of claim 1 wherein after the CMP process, the method further comprises the following steps:

depositing a silicon layer over the semiconductor substrate;

coating and patterning an etch support (ES) photoresist layer on the silicon layer, the ES photoresist layer masking the vertical transistor memory array region and a

portion of the transition region;
etching the silicon layer using the ES photoresist layer as a hard mask to define an array etch mask; and
stripping the ES photoresist layer.

[c3] 3.The method of claim 2 wherein after stripping the ES photoresist layer, the method further comprises the following steps:
using the array etch mask to protect the vertical transistor memory array region and removing the second pad nitride and second oxide in the support region, thereby exposing the support active areas;
performing a thermal oxidation process to grow a sacrificial oxide layer on the exposed support active areas; and
removing the array etch mask.

[c4] 4. The method of claim 2 wherein the silicon layer is polysilicon layer.

[c5] 5.The method of claim 2 wherein the silicon layer is amorphous silicon layer.

[c6] 6. The method of claim 1 wherein the vertical transistor memory cell comprises a storage node, trench top oxide (TTO), and polysilicon gate of the vertical transistor, and wherein the TTO is used to isolate the storage node from

the polysilicon gate of the vertical transistor.

[c7] 7. The method of claim 1 wherein before depositing the protective dielectric layer, HFEG (hydrofluoric ethylene glycol) is used to etch away a predetermined thickness of the second pad nitride.

[c8] 8. The method of claim 7 wherein the predetermined thickness of the second pad nitride is 50~200 angstroms.

[c9] 9. A method for fabricating a vertical transistor DRAM device, comprising:
providing a semiconductor substrate comprising a vertical transistor memory array region, a support region, and a transition region between the vertical transistor memory array region and the support region, wherein the vertical transistor memory array region comprises a plurality of array active areas, the support region comprises a plurality of support active areas, and wherein a first pad oxide and a first pad nitride are formed on each of the array active areas, and a second pad oxide and second pad nitride are formed on each of the support active areas;
depositing a protective dielectric layer over the semiconductor substrate;
coating and patterning an etch array (EA) photoresist

layer on the protective dielectric layer, so that the EA photoresist layer masking the support region and a portion of the transition region;

using the EA photoresist layer as an etching mask and etching the protective dielectric layer to expose the first pad nitride in the vertical transistor memory array region;

stripping the EA photoresist layer;

removing the first pad nitride in the vertical transistor memory array region to form recesses on the array active areas;

depositing a dielectric layer covering the protective dielectric layer on the support region, the vertical transistor memory array region, and the transition region, and the dielectric layer filling the recesses;

performing a chemical mechanical polishing (CMP) process to polish the dielectric layer and the protective layer on the support region using the second pad nitride as a polishing stop layer;

depositing a silicon layer over the semiconductor substrate;

coating and patterning an etch support (ES) photoresist layer on the silicon layer, the ES photoresist layer masking the vertical transistor memory array region and a portion of the transition region;

etching the silicon layer using the ES photoresist layer as

a hard mask to define an array etch mask; and
stripping the ES photoresist layer.

[c10] 10. The method of claim 9 wherein after stripping the ES photoresist layer, the method further comprises the following steps:
using the array etch mask to protect the vertical transistor memory array region and removing the second pad nitride and second oxide in the support region, thereby exposing the support active areas;
performing a thermal oxidation process to grow a sacrificial oxide layer on the exposed support active areas; and
removing the array etch mask.